REMARKS

The Office Action mailed on July 17, 2001, has been received and reviewed. Claims 31-35 and 37-45 are currently pending in the application. Claims 31-35 and 37-45 stand rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 102

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Ahn

Claims 31-35, 37, 38, and 40-45 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,358,888 to Ahn et al. (hereinafter "Ahn").

Ahn discloses, among other things, a semiconductor capacitor structure that includes a capacitor electrode that includes a base and a plurality of laterally isolated islands extending upwardly therefrom. As such, the capacitor electrode of Ahn could be said to include a recesses extending downwardly between the islands.

Independent claim 31 recites a semiconductor capacitor storage poly that includes downwardly extending recesses and a plurality of "contiguous" mesas forming a "maze-like" structure. It is well known that the term "contiguous" refers to structures that touch one another, that share a boundary, or that are connected without a break therebetween. *See, e.g.,* The American Heritage College Dictionary, 3d ed. (Houghton, Mifflin 1997).

Ahn also discloses an intermediate structure, which is illustrated in FIG. 14 thereof, that includes recesses formed in a conductive layer 40b and that separate sections 40c of conductive

layer 40b. These recesses are also located laterally between elevated regions of the HSG layer 80 (*see,* col. 8, lines 32-35, which indicates that HSG layer 80 is used as an etch mask to pattern first material layer 50b and that the patterned first material layer 50c is, in turn, used as a mask for the patterning of conductive layer 40b).

Rather than teach a capacitor structure with "contiguous" elements that form a "maze-like" structure, the islands of the capacitor structure disclosed in Ahn are laterally isolated from one another.

For this reason, it is respectfully submitted that Ahn does not expressly or inherently disclose each and every element of claim 31. Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(b), claim 1 is allowable over Ahn.

Claim 32 is allowable, among other reasons, for depending from claim 31, which is allowable.

Independent claim 33 recites a semiconductor capacitor storage poly that includes downwardly extending recesses and a plurality of "contiguous" webs forming a "maze-like" structure. Independent claim 33 also recites that the semiconductor capacitor storage poly may include hemispherical-grain polysilicon on tup surfaces of at least ome of the plurality of contiguous webs.

By way of contrast with claim 33, Ahn discloses a capacitor structure that includes laterally distinct islands, not a capacitor that includes "contiguous" webs that form a "maze-like" structure.

It is, therefore, respectfully submitted that Ahn does not expressly or inherently disclose each and every element of claim 33 and that, under 35 U.S.C. § 102(b), claim 33 is allowable over Ahn.

Claim 34 is allowable, among other reasons, as depending from claim 33, which is allowable.

Independent claim 35 recites an intermediate semiconductor capacitor structure that includes a storage poly with recesses formed therein, a hemispherical-grain polysilicon layer of the storage poly structure, and a mask over the hemispherical-grain polysilicon layer. Claim 35 also recites that the recesses are exposed through the hemispherical-grain polysilicon layer and the mask.

In contrast, Ahn lacks any express or inherent disclosure of a mask over the hemispherical-grain polysilicon layer thereof. Rather, it is the hemispherical-grain polysilicon layer of Ahn that forms an etch mask through which the underlying storage structure is formed, with recesses in the storage structure being formed beneath locations where low-elevation regions of the hemispherical-grain polysilicon layer were previously formed.

Further, Ahn fails to disclose, either expressly or inherently, that any hemispherical-grain polysilicon would remain on the storage poly structure and that recesses formed in the storage poly structure could be exposed therethrough. Specifically, if the storage structure of Ahn were formed from polysilicon as is required by the recitation of "storage poly structure" in claim 35, it would be necessary to completely remove the hemispherical-grain polysilicon from above a storage structure formed from polysilicon to directly or indirectly form recesses of adequate depth therein.

For these reasons, it is respectfully submitted that Ahn does not expressly or inherently disclose each and every element of claim 35. It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(b), claim 35 is allowable over Ahn.

Independent claim 37 recites an intermediate semiconductor memory cell structure that includes a storage poly, low elevations regions of a hemispherical-grain polysilicon layer on the storage poly structure, recesses formed in the storage poly structure laterally between the low elevation regions of the hemispherical-grain polysilicon layer, and dielectric layer lining the recesses.

While Ahn discloses a memory cell storage structure that includes recesses extending downwardly therein and that these recesses may be lined with dielectric material, Ahn lacks any express or inherent disclosure that the recesses of the storage structure could be located laterally between low elevation regions of a hemispherical-grain polysilicon layer. Rather, since Ahn discloses that hemispherical-grain polysilicon is itself employed as an etch mask to form a storage structure, any low elevation regions thereof would be etched away before higher elevation regions thereof. Thus, recesses of the resulting storage structure would be formed directly beneath positions where the low elevation regions of the hemispherical-grain polysilicon were previously located. Therefore, the recesses of the storage structure could not be located laterally between low elevation regions of a hemispherical-grain polysilicon layer, as is recited in independent claim 37.

Accordingly, it is respectfully submitted that Ahn does not expressly or inherently disclose each and every element of independent claim 37. Therefore, it is respectfully submitted that, under 35 U.S.C. § 102(b), claim 37 is allowable over Ahn.

Independent claim 38 recites a semiconductor memory cell structure that includes a storage poly structure, regions of hemispherical-grain polysilicon on at least portions of an upper surface of the storage poly structure, and recesses extending into the storage poly structure. At least some of the recesses are located laterally between the regions of hemispherical-grain polysilicon. The semiconductor memory cell structure of claim 38 also includes a dielectric layer substantially coating an upper surface of the storage poly structure and substantially lining each of the plurality of recesses.

In contrast to claim 38, Ahn lacks any express or inherent disclosure of a semiconductor memory cell structure that includes a storage poly structure with hemispherical-grain polysilicon on an upper surface thereof. Rather, since Ahn discloses that hemispherical-grain polysilicon is used as an etch mask to directly or indirectly form islands of the disclosed storage structure, in order to form a storage structure with recesses of adequate depth from polysilicon, as is required

by the recitation of "storage poly structure" in claim 38, it would have been necessary in the process described in Ahn to etch all of the hemispherical-grain polysilicon layer away from the underlying material of the storage structure.

Accordingly, it is respectfully submitted that Ahn does not expressly or inherently disclose each and every element of claim 38 and that claim 38 is, therefore, allowable under 35 U.S.C. § 102(b).

Claims 40 and 41 are both allowable, among other reasons, as depending from claim 38, which is allowable.

Independent claim 42 recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a substantially confluent hemispherical-grain polysilicon layer on the storage poly structure, and a mask positioned over the substantially confluent hemispherical-grain polysilicon layer. Claim 42 also recites that elevated portions of the hemispherical-grain polysilicon layer are exposed through the mask.

Assuming, *arguendo,* that element 70 of FIG. 18 of Ahn could be a mask, as is recited in claim 42, Ahn still lacks any express or inherent disclosure that elevated regions of the hemispherical-grain polysilicon described therein are exposed through element 70.

It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(b), claim 42 is allowable over Ahn.

Independent claim 43, as amended and presented herein, recites an intermediate semiconductor capacitor structure that includes a storage poly structure with recesses formed therein, portions of a hemispherical-grain polysilicon layer substantially overlying upper portions of the storage poly structure, and a mask positioned over the hemispherical-grain polysilicon layer. The mask is spaced apart from the storage poly structure by way of the hemispherical-grain polysilicon layer and positioned laterally between recesses formed in the storage poly structure.

Ahn lacks disclosure of a storage poly structure that has portions of a hemispherical-grain polysilicon layer on upper portions thereof, as well as of a mask that is positioned laterally between recesses formed in the storage poly structure and that is spaced apart from a storage poly structure which includes recesses formed therein by way of the hemispherical-grain polysilicon layer. Rather, element 70, the only element disclosed in Ahn as a mask that overlies the polysilicon layer disclosed therein, is located only around the outer periphery of the storage structure, not laterally between recesses formed in the underlying storage structure.

Accordingly, it is respectfully submitted that Ahn does not expressly or inherently disclose each and every element of amended claim 43, as is required to maintain a rejection under 35 U.S.C. § 102(b).

Independent claim 44, as amended and presented herein, recites an intermediate semiconductor capacitor structure that includes a storage poly structure with recesses formed therein, a hemispherical-grain polysilicon layer on at least portions of the storage poly structure, and a mask that overlies at least portions of the hemispherical-grain polysilicon layer that are located laterally between the recesses formed therein. The intermediate semiconductor capacitor structure of claim 44 also includes dielectric material lining the recesses.

Again, Ahn lacks any express or inherent disclosure of an intermediate semiconductor capacitor structure that includes hemispherical-grain polysilicon laterally between recesses formed in a storage structure or of a mask that overlies such hemispherical-grain polysilicon.

As Ahn does not expressly or inherently disclose each and every element of amended independent claim 44, it is respectfully submitted that, under 35 U.S.C. § 102(b), claim 44 is allowable over Ahn.

Independent claim 45 recites an intermediate semiconductor memory cell structure that includes a storage poly structure with recesses formed therein, low elevation regions of a hemispherical-grain polysilicon layer on at least portions of the storage poly structure, and a

mask that overlies at least the low elevation regions of the hemispherical-grain polysilicon layer. The recesses formed in the storage poly structure of claim 45 are exposed between the low elevation regions of the hemispherical-grain polysilicon layer and through said mask. Claim 45 also recites that dielectric material lines the recesses.

As Ahn lacks express or inherent disclosure of an intermediate semiconductor memory cell structure that includes a storage poly structure with recesses formed therein and exposed through a mask and between low elevation regions of a hemispherical-grain polysilicon layer, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 45 is allowable over Ahn.

Batra

Claims 38-41 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,060,355 to Batra et al. (hereinafter "Batra").

Batra teaches a process for forming rough silicon layers. Among other things, Batra discloses and, in FIG. 6, illustrates a DRAM cell 85 that includes a bottom electrode comprising a substrate 50 and a rough layer 86. The rough layer 86 is formed from hemispherical-grain polysilicon. It has also been asserted in the outstanding Office Action that low elevation regions of the hemispherical-grain polysilicon of rough layer 86 comprise recesses therein.

Independent claim 38 recites a memory cell structure that includes, among other things, a storage poly structure and regions of hemispherical-grain polysilicon on at least portions of an upper surface of the storage poly structure. In addition, a plurality of recesses extend into the storage poly structure of claim 38.

By way of contrast with claim 38, the purported recesses of the DRAM cell described in Batra are limited to the low elevation regions of the hemispherical-grain polysilicon rough layer 86. Batra does not expressly or inherently describe that these recesses may extend into the underlying substrate 50, which, in the Office's estimation, is apparently analogous to the storage poly structure recited in claim 38.

As Batra does not expressly or inherently describe each and every element of independent claim 38, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 38 is allowable over Batra.

Each of claims 39-41 is allowable, among other reasons, as depending from claim 38, which is allowable.

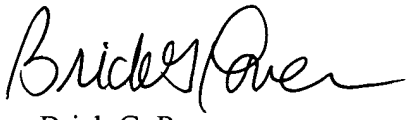
Claim 40 is further allowable since Batra does not expressly or inherently describe a poly cell structure that comprises a "web-like" structure. Rather, the substrate 50 of Batra appears to be a solid layer of material.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(b) rejections of claims 31-35 and 37-45 be withdrawn.

CONCLUSION

Each of claims 31-35 and 37-45 is believed to be in condition for allowance. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the case has been passed for issuances. If any issues preventing the allowance of any of claims 31-35 and 37-45 remain which might be resolved by way of a telephone conference, the Office is respectfully invited to contact the undersigned attorney.

Respectfully Submitted,



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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 40, 43, and 44 as follows:

40. (Amended) The semiconductor memory cell structure of claim 38, wherein said storage poly structure [has] comprises a web-like structure.

43. (Twice amended) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure including recesses formed therein;

portions of a hemispherical-grain polysilicon layer [on at least] substantially overlying upper portions of said storage poly structure; and

a mask positioned over said hemispherical-grain polysilicon layer, laterally between said recesses, and spaced apart from said storage poly structure by said hemispherical-grain polysilicon layer, said recesses in said storage poly structure being exposed through said mask.

44. (Amended three times) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure with recesses formed therein;

a hemispherical-grain polysilicon layer on at least portions of the storage poly structure;

a mask overlying at least portions of said hemispherical-grain polysilicon layer located laterally between said recesses; and

dielectric material lining at least said recesses.